SF100
Serial Flash Programmer
Specification
V2.3

The Innovative solution to update the Serial Flash on board

- **High performances of low price**
- **USB full speed support**
- **In Circuit Programming (program on board SPI Flash)**
- **Socket Programming (program SPI flash in the socket)**
- **ICP connector to work with Serial Flash soldered on board**
- **Friendly and powerful tool with free life time update via Website**
- **Portable programmer:**
  - **SF100: (10cm X 5cm X 2 cm)**
- **Advanced I/O control**

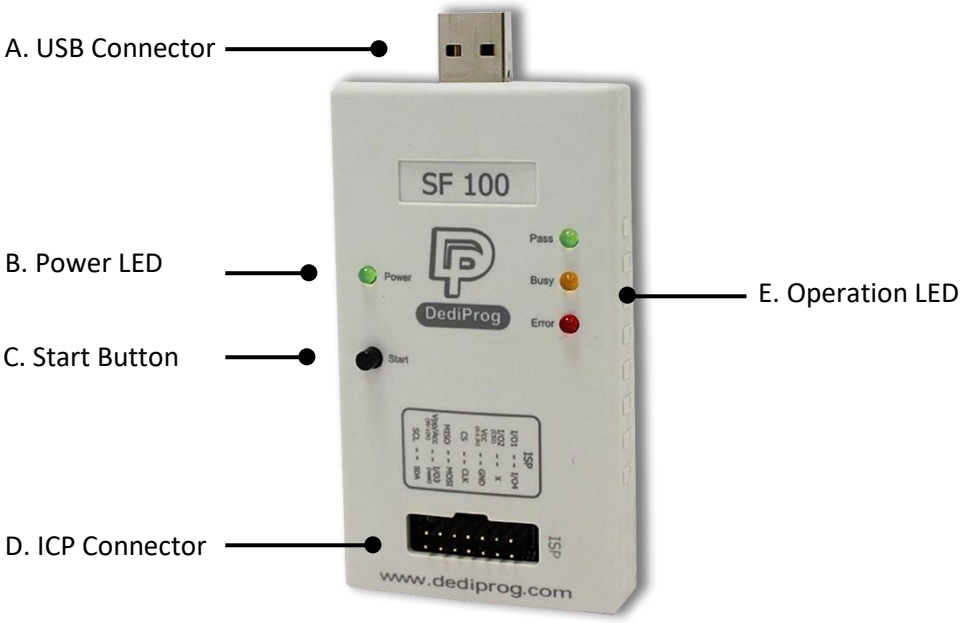
Table of Content

I. Product Description

The SF100 programmers are used to read, program or update the Serial Flash soldered on board or inserted in the socket of the DediProg Backup Boot Flash tool by using the computer software through USB communication.

1.1 Interface description

Fig 1: SF100 Programmer



A. USB Connector

Connect the programmer to the computer.
A USB cable extension is provided for more flexibility and convenience.

B. Power LED

Power LED will shine when SF100 is powered by USB.

C. Start button

Start operations from the programmer

D. ICP Connector

Connect the SPI signals and power supply to the application Serial Flash via a flat cable. The flat cable is flexible and convenient to manipulate, and can be changed easily before connection. For customization of the ICP-cable (number of signals, pin out assignment or connector size), please contact DediProg.

E. Operation LED

- Red Led: error
- Orange Led: operation on going
- Green Led: pass

1.2 Connected to the application pin header

The SF100 programmer has been designed to meet the strong and growing demand of serial flash users to program and update the memories soldered on board during development, production, and field manipulation or repairing with high performance and low cost. Before trying to update the Serial Flash on Board, be sure that the SPI controller and the application are compatible with the In Circuit Programming method to avoid any conflict with the programmer.

DediProg has published Application Note to help designers to implement the ICP method and will be pleased to answer to any of your questions on this subject.

Fig 2: SF100 connected to the application pin header

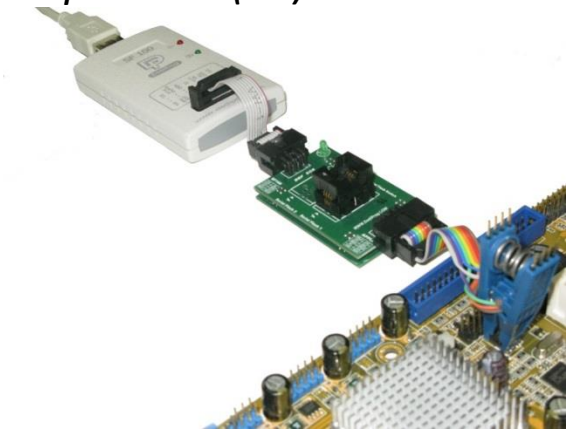
1.3 Connected to Backup Boot Flash

The software provided with the SF100 has been developed to offer a complete portfolio of features with a friendly and simple interface to not require any technical expertise.

SF100 can also be used together with DediProg backup boot flash modules so that it forces the application to boot from the backup flash located in the backup boot flash module instead of the soldered SPI flash on the application.

The backup serial flash can then be accessed at any time with the SF100 without any possible conflict with the application controller.

Fig 3: Backup Boot Flash (BBF) connected to SF100

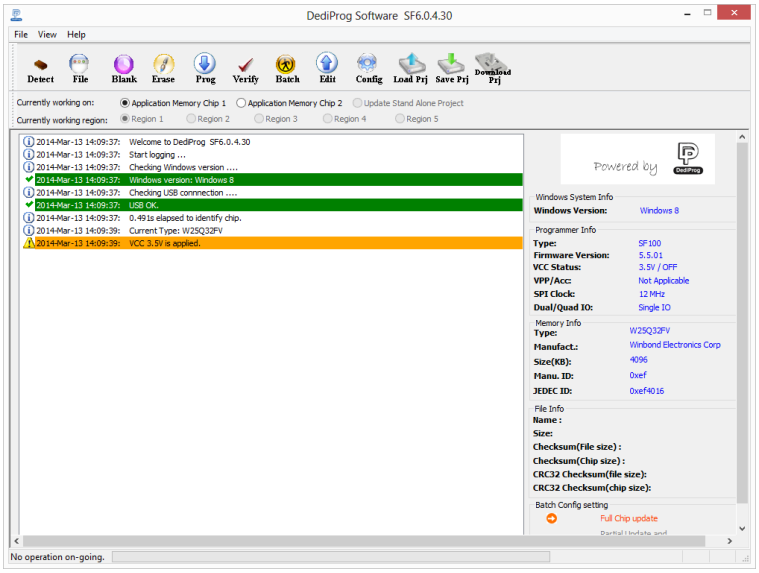


II. Products Features

2.1 USB mode

In USB mode, user can control the programmer operations via a friendly interface.
User can load a file, blank check, program and verify the target Serial Flash. Batch button provides an easy way to perform more than one operation in one click.
User can also edit the buffer, files and SPI Flash content and compare.

Fig 4: USB Window interface

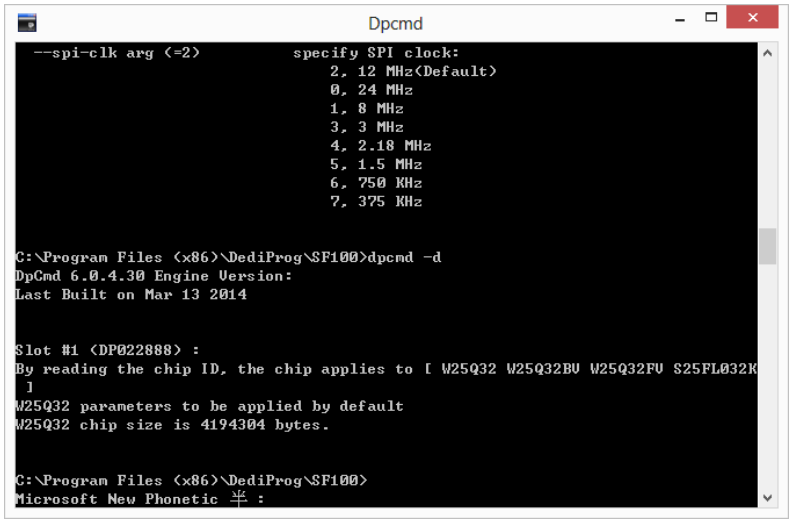


To get more information on the software features, please refer to our user manual.

2.2 Command line mode

User can quickly perform some repetitive operations just by typing the command on our Dpcmd interface or control programmer using other software (compiler or ICT tester).

Fig 5: Dpcmd interface



III. Specification

3.1 USB Connector

The USB connector type A is available to communicate with the computer tool.

USB Power supply specification:
- Vdd = 5V ± 5%
- Idd min = 500mA

3.2 DC and IO characteristics

3.2.1 ICP DC and AC characteristics

The ICP connector is a 7x2 pin header straight type with 2.54mm pitch. It is used to control the application SPI Flash, and if necessary supply the SPI Flash, provide the high voltage to the SPI Flash, or reset the application chipset, etc.

Table 1: SF100 connector Pin out:

1	I/O1	I/O4	**2**
3	I/O2 or CS2	NC	**4**
5	Vcc	GND	**6**
7	CS	CLK	**8**
9	MISO	MOSI	**10**
11	Vpp/Acc	I/O3	**12**
13	SCL	SDA	**14**

Table 2: Description of the signals:

Pin Number	Name of the signals	Description
1,2,3,12	General I/O	General I/O are used to control optional pins of the SPI Flash (hold, WP) or switch the application to a specific mode (reset chipset or switch OFF MOSFET)
3	I/O2	I/O2 can also been used as a second Chip Select (CS2) to update two serial Flashes on the board (option selected from the DediProg software). *
4	NC	Not Connected
5	Vcc	Vcc is used to supply the application SPI Flash
6	GND	GND is the common ground shared between application and programmer
7	CS	SPI chip select of the application SPI Flash
8	CLK	SPI clock signal for the application SPI Flash
9	MISO	Data out from the application memory (master in slave out)
10	MOSI	Data in of the application SPI Flash (master out slave in)
11	Vpp	High voltage applied on the SPI Flash to speed up the programming and erasing operations
13,14	SCL, SDA	I2C bus reserved for future use

* Available on the products with firmware 2.x.x and after

A. Application SPI Flash supply: Vcc

Specification for the ICP Vcc pin:

- Vcc is set at 3.3V by default and can be switched to 2.5V or 1.8V on the hardware version 3 and after (hardware version can be identified with the firmware version V3.xx)
- Icc max supplied = 50mA

The application SPI Flash can be supplied by two different sources:

a) by the programmer via ICP Vcc pin
b) by the application according to the SPI Flash specification

B. SPI signals management: CS, CLK, MISO and MOSI

The SPI signals are used to communicate with the application SPI Flash with a high frequency (24MHZ or 12MHZ according to the firmware). The frequency can be also adjusted on the latest hardware. The signals are CMOS compatible and are switched in High Impedance when not used.

Table 3: DC specification for SPI signals and IO

Symbol	Parameter	Test condition		Value	Unit
		Vcc(V)	Io(mA)		
Vih	High Level Input Voltage	2.7V to 3.6V		2V	V min
		2.3V to 2.7V		1.7V	V min
		1.65V to 1.95V		0.65XVcc	V min
Vil	Low Level Input Voltage	2.7V to 3.6V		0.8V	V max
		2.3V to 2.7V		0.7V	
		1.65V to 1.95V		0.35XVcc	
Ioh	High Level Output current	3V	-24mA		mA
		2.7V	-12mA		mA
		2.3V	-12mA		mA
		1.65V	-4mA		mA
Iol	Low Level Output current	3V	24mA		mA
		2.7V	12mA		mA
		2.3V	12mA		mA
		1.65V	4mA		mA
Cap	Capacitance			10nF	nF typ

This specification is relative to individual capability of one signal.

ESD high performance protection compliant with IEC61000-4-2 level 4:
15kV (air discharge)
8kV (contact discharge)

Remark: the total capacitance added on the application SPI bus will also depend on the ICP cable length. The ICP cable length must be reduced at the minimum. The SPI flash output buffer capability (MISO) is limited compared to the programmer performances. So even if the programmer is able to drive high capacitance, the Serial Flash soldered on the application will probably not (information read from SPI Flash will be wrong).

C. Smart management of the SPI Flash Vcc and SPI signals

In order to minimize the impact of the ICP method on the chipset and application board, the programmer supplies the application Serial Flash with Vcc and SPI signals only during the programmer and Serial Flash operations.

Advantages:

a) The programmer is plugged on the application board with Vcc OFF and SPI signals in High Impedance to avoid inrush current.

b) All the ICP pins are protected with ESD high performance protections to discharge the Electronics charge before the connection and protect the application.

c) The Serial Flash Vcc and SPI signals are provided only when the user send the command and are switched OFF automatically when the operation is completed. Therefore, the programmer is transparent for the application and can be kept connected during application trials.

D. High voltage supply: Vpp/Acc

Specification for the Vpp pin

Vpp = 8.5V to 12.5V

Ipp max = 50mA

The Vpp high voltage can be supplied by the programmer and used to speed up programming and erasing of the application Serial Flash if this feature is supported by the Serial Flash supplier.

The Vpp supply will be applied automatically by the programmer on the Vpp pin only during erase, write, or programming operations and only if the Vpp option has been enabled on the software. The programmer will also control the Vpp voltage level according to the Serial Flash connected and its specification.

E. I/O management: I/O1, I/O2, I/O3, I/O4

Four general outputs are available on the ICP connector for custom needs. The IOs are in HZ state if there is no software operation ongoing even if the power is connected. The IOs are driven high or low when the software is running command.

I/O4, I/O2 = driven High
I/O1, I/O3 = driven Low

These outputs can be useful to drive Wp, Hold, reset the application chipset, or switch Off the MOSFET transistors in the application board. They are CMOS compatible and are switched in High Impedance when the software is not executing commands.

The **I/O2** can also be used as a s**econd Chip Select** to update a second SPI Flash soldered on the board. In this case, I/O2 have to be connected to the application CS2 and the option “Chip 2” has to be selected in the DediProg software.

For the DC characteristics please refer to table 3.

ESD high performance protection compliant with IEC61000-4-2 level 4:

15kV (air discharge)

8kV(contact discharge)

3.2.2 ICP timing

The IO has been designed to set the application in external programming mode before applying the SPI signal. They can be used to reset the chipset and application, to drive multiplexers and switch SPI bus from application controller to programmer, to turn off MOSFET and isolate the SPI bus when programmer is working.

This is the behavior of the IO and SPI signals on our latest firmware.

A. If No programmer operation is on going

All our SF100 outputs are equivalent to high impedance.

B. When an operation is requested on the user interface

- I/O1, I/O2, I/O3 and I/O4 are first switched in Low impedance
- I/O1 and I/O3 are driven low
- I/O2 and I/O4 are driven high

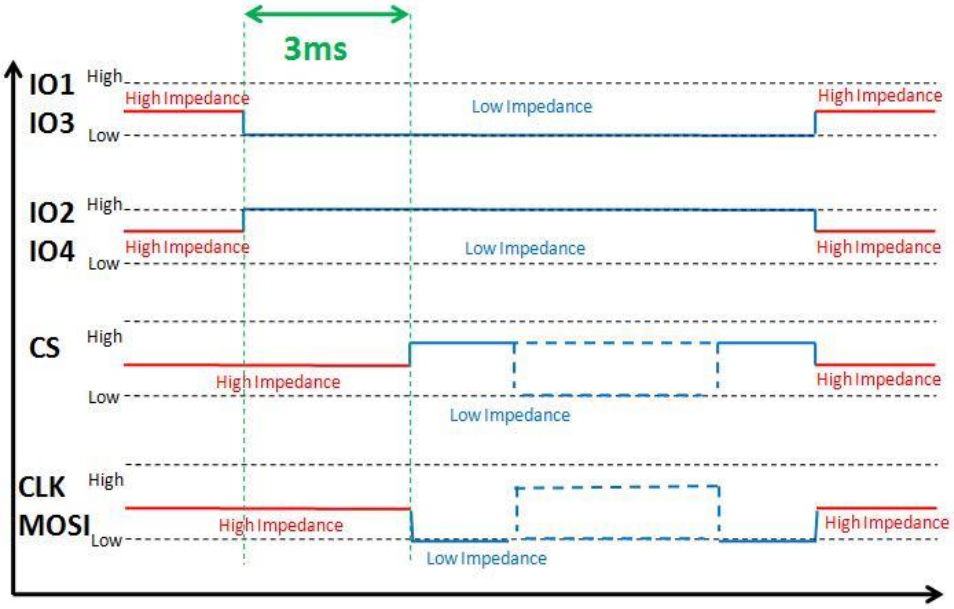
C. 3ms after IO are switched to Low Impedance, the CS, Clock and MOSI outputs are switched in low impedance too.CS1 and CS2 are driven high

- CS is driven high
- Clock and MOSI are driven low.

D. The programmer is then ready for the communication with the Serial Flash.

So designer can use I/O3 to reset or switch the application in external programming mode. Application will have a delay of 3ms between I/O3 is driven low and Programmer SPI outputs are switched from High Impedance to Low Impedance. SPI communication starts 6ms after I/O3 has been driven low.

Fig 6: IO and SPI timing



3.2.3 Host PC requirements

The SF100 interface with IBM compatible PC's through the USB 2.0/1.1 port. This gives full compatibility with the latest PC's, notebooks and portables.

System Requirements:

- PC with Windows XP / Vista / 7 / 8 / 8.1
- Hard disk with at least 64 MB free space.

System Interface:

- PC connexion ……..USB 2.0/1.1 port

IV. Programming Performance

Table 4: Programming and verify in USB mode

SPI Flash Densities	8 Mbit	16 Mbit	32 Mbit	64 Mbit	128 Mbit	256 Mbit	512Mbit	1Gbit
Program+ Verify	11s	15s	20.5s	48.5s	94s	157s	297s	717s
Reference IC	W25X80VSSIG	W25Q16VSSIG	W25Q32FVSSIG	W25Q64CVSSIG	W25Q128BVFIG	W25Q256FVFG	S25FL512SAIF01	N25Q00AA13GSF40

Note 1: The measurements are done with SF100 with firmware 5.5.01 and software version of 6.0.4.28. The tested memories are from a single serial flash manufacturer.

Note 2: new hardware versions with firmware 3.x.x allow Vpp/Acc high speed programming if the chip supports it. The programming performance will be better if applying Vpp/Acc during the programming or erasing for chips supporting such feature.

V. Revision History

Date	Version	Changes
2010/05/17	V1.0	1. SF100 and SF200 updated with 3 LED and Start button. 2. System requirements updated.
2014/03/13	V2.0	1. Remove SF200/SF300. 2. Software interface updated.
2016/03/14	V2.2	VCC description changed.
2017/07/28	V2.3	Modified document formats and changed company address.

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